

REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

No claims are currently being cancelled.

Claims 1, 8-10, 12, 14 and 19 are currently being amended.

No claims are currently being added.

This amendment and reply amends claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-21 are pending in this application.

Interview with Examiner Salerno:

Applicants' representative appreciates the courtesies extended to him during a telephone interview conducted on December 9, 2008, in which a draft response was discussed. In response to a question posted by Examiner Salerno concerning a feature in claim 12 concerning the drain electrode side being lower than a gate electrode side in a dielectric constant of a capacity, please refer to Figure 5 of the drawings and the description of that figure in the specification, as well as to the attached Exhibit 2 to this amendment and reply, which is discussed below with reference to claim 12.

Claim Rejections – Prior Art:

In the Office Action, claims 9 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent Application JP 09-307097 to Kawai; claims 1-6, 8, 10, 11 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Japanese Patent Application JP 2000-323495 to Tsukino; claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Tsukino and further in view of U.S. Patent Publication No. 2003/0020092 to Parikh et al.; claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Tsukino and further in view of

U.S. Patent No. 6,483,135 to Mizuta et al.; claims 14 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Tsukino and further in view of U.S. Patent Publication 2001/0015446 to Inoue et al.; claims 16 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Tsukino and further in view of U.S. Patent Publication No. 2001/0017370 to Sheppard et al.; and claims 19-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kawai in view of Tsukino and further in view of U.S. Patent Publication No. 2002/0043697 to Hirokawa. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

Independent Claim 9:

In its rejection of claim 9, the Office Action asserts that insulating film 5 of Kawai as shown in Figure 4 of that reference has dielectric constants not more than 3.5. However, the insulating film 15 of Kawai is a SiO₂ film. The dielectric constants of a SiO₂ film is 3.9, as shown in the attached Exhibit 1 to this amendment and reply.

Accordingly, since Kawai does not disclose or suggest an insulating film having dielectric constants not more than 3.5, whereby 3.9 is greater than 3.5, presently pending independent claim 9 is not anticipated by Kawai.

Independent Claim 12:

Kawai (the only reference cited against claim 12) does not disclose or suggest that a drain electrode side is lower than a gate electrode side in a dielectric constant of a capacity formed by a field plate portion, a Group III nitride semiconductor layer and an insulating film sandwiched therebetween. Rather, in Kawai, the dielectric constant of a capacity formed by a field plate portion, a Group III nitride semiconductor layer and an insulating film sandwiched therebetween is uniform, because the insulating film 15 of Kawai consists of one SiO₂ layer, as seen in Figure 4 of Kawai. Thus, Kawai discloses that the dielectric constant of a capacity of a drain electrode side is equal to (and thus not lower than) the dielectric constant of a capacity of a gate electrode side.

In response to the query posed by Examiner Salerno in the telephone interview conducted on December 9, 2008, as shown in Figure 5 of the drawings and as described in

Example 5 of the specification, the first area and the second area are formed by a single-layer of a SiN film 21. The second area is positioned on the drain side, and is formed by laminating the SiO₂ film 22 on the SiN film 21. The drain electrode 3 side is lower than the gate electrode 2 side in the dielectric constant of the insulating film below the field plate portion 5. As such, the drain electrode side and the gate electrode side in the area near the field plate portion do not have the same dielectric constant. The attached Exhibit 2, which corresponds to a marked-up version of Figure 5 of the drawings, shows this feature.

Accordingly, presently pending independent claim 12 is not anticipated by Kawai.

Claims 1-8, 10, 11 and 13-21:

Claims 1-8, 10, 11 and 13-21 are rejected over the combination of Kawai and Tsukino. However, it is respectfully submitted that one of ordinary skill in the art would not combine the teachings of Kawai and Tsukino, for the reasons given below.

The transistor of Tsukino is a JFET, which is formed by diffusing an impurity in the substrate to make a drain region, a source region, a channel region and a P+ region. Controlling the depletion layer formed by the P+ region and the channel region drives the transistor of Tsukino, whereby a protective film 32 consisting of an SiN film and an SiO₂ film is used to inhibit impurity diffusion depth variation of the P+ region.

On the contrary, the transistor of Kawai is a MESFET, as shown in Figure 4 of Kawai. Controlling the depletion layer formed by a Schottky barrier between a gate metal and a semiconductor layer drives the transistor of Kawai. Thus, the transistor of Kawai does not have an impurity diffusion region.

As clearly seen from the above discussions of Tsukino and Kawai, it is difficult to provide a protective film 32 of Tsukino on the transistor of Kawai, because the protective film 32 is for inhibiting impurity diffusion depth variation, whereby Kawai does not have an impurity diffusion region.

Accordingly, since Tsukino and Kawai cannot be combined in the manner suggested in the Office Action, claims 1-6, 8, 10, 11 and 15 are patentable over the cited art of record. Claims 13, 14 and 16-21 are also patentable because the other cited art of record does not

does not change the above arguments concerning the inability to combine the teachings of Tsukino with those of Kawai.

Furthermore, claims 1-8, 10, 11 and 13-21 are directed to an HJFET (heterojunction FET), which has excellent characteristics for a balance between a collapse and a gate breakdown voltage, whereby such characteristics are not taught or suggested by either Tsukino or by Kawai.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorize payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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